IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellant: Robert J. Schultz
Group Art Unit: 2467
Application No.: 10/809,164
Examiner: Choi, Eunsook
Filed: March 25, 2004
Confirmation No.: 7766

For: PROCESSING PACKET INFORMATION USING AN ARRAY OF PROCESSING ELEMENTS

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REPLY BRIEF UNDER 37 C.F.R. § 41.41(a)

This is an appeal to the Board of Patent Appeals and Interferences from the decision of the Examiner dated March 9, 2009, which finally rejected claims 1-15, 17, 18, 20, and 21 in the above-identified application. The Office date of receipt of Appellant's Notice of Appeal was June 9, 2009. An Appeal Brief was filed on August 6, 2009. This Reply Brief is in response to the Examiner's Answer dated October 26, 2009. This Reply Brief is hereby submitted pursuant to 37 C.F.R. § 41.41(a).

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Date:_____ Signed:_____

Typed Name: Jeffrey T. Holman

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I. STATUS OF CLAIMS

Claim 19 is canceled.

No claims are withdrawn.

Claim 16 was objected to as being dependant upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1-15, 17, 18, 20, and 21 stand rejected as follows:

Claim 12 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Key et al. (U.S. Pat. No. 6,272,621, hereinafter Key) in view of Rhoades et al. (U.S. Pat. Pub. No. 2003/0041163, hereinafter Rhoades).

Claims 1, 2, and 3 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rhoades in view of Van Lunteren et al. (U.S. Pat. No. 7,193,997, hereinafter Van Lunteren).

Claims 6, 7, 11, 14, and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Key in view of Rhoades and Van Lunteren.

Claims 13, 17, 18, 20, and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Key in view of Rhoades and Kaganoi et al. (U.S. Pat. Pub. No. 2003/0012198, hereinafter Kaganoi).

Claims 4 and 5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rhoades modified by Van Lunteren and further in view of Khanna (U.S. Pat. No. 7,219,187, hereinafter Khanna).

Claim 10 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Key modified by Rhoades and Van Lunteren and further in view of Khanna.

Claims 8 and 9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Key modified by Rhoades and Van Lunteren and further in view of Kaganoi.

Claims 1-15, 17, 18, 20, and 21 are the subject of this appeal. A copy of claims 1-15, 17, 18, 20, and 21 is set forth in the Claims Appendix.

II. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claim 12 is patentable over the combination of Key and Rhoades under 35 U.S.C. 103(a).

B. Whether claims 1, 2, and 3 are patentable over the combination of Rhoades and Van Lunteren under 35 U.S.C. 103(a).

C. Whether claims 6, 7, 11, 14, and 15 are patentable over the combination of Key, Rhoades, and Van Lunteren under 35 U.S.C. 103(a).

D. Whether claims 13, 17, 18, 20, and 21 are patentable over the combination of Key, Rhoades, and Kaganoi under 35 U.S.C. 103(a).

E. Whether claims 4 and 5 are patentable over the combination of Rhoades, Van Lunteren, and Khanna under 35 U.S.C. 103(a).

F. Whether claim 10 is patentable over the combination of Key, Rhoades, Van Lunteren, and Khanna under 35 U.S.C. 103(a).

G. Whether claims 8 and 9 are patentable over the combination of Key, Rhoades, Van Lunteren, and Kaganoi under 35 U.S.C. 103(a).

III. ARGUMENT

For the purposes of this appeal, claim 12 is argued separately for purposes of the question of patentability over combination of Key and Rhoades under 35 U.S.C. 103(a). Claims 1, 2, and 3 are argued together as a separate group for purposes of the question of patentability over the combination of Rhoades and Van Lunteren under 35 U.S.C. 103(a). Claims 6, 7, 11, 14, and 15 are argued together as a separate group for purposes of the question of patentability over the combination of Key, Rhoades, and Van Lunteren under 35 U.S.C. 103(a). Claims 13, 17, 18, 20, and 21 are argued together as a separate group for purposes of the question of patentability over the combination of Key, Rhoades, and Kaganoi under 35 U.S.C. 103(a). Claims 4 and 5 are argued together as a separate group for purposes of the question of patentability over the combination of Rhoades, Van Lunteren, and Khanna under 35 U.S.C. 103(a). Claim 10 is argued separately for purposes of the question of patentability over the combination of Key, Rhoades, Van Lunteren, and Khanna under 35 U.S.C. 103(a). Claims 8 and 9 are argued together as a

separate group for purposes of the question of patentability over the combination of Key, Rhoades, Van Lunteren, and Kaganoi under 35 U.S.C. 103(a).

A. Claim 12 is patentable over the combination of Key and Rhoades because the combination of cited references does not teach all of the limitations of the claim.

Appellant respectfully submits that claim 12 is patentable over the combination of Key and Rhoades because the combination of references does not teach all the limitations of the claim. Claim 12 recites:

> A system for processing packet information comprising:
> an array of processing elements having;
> at least one first stage processing element; and
> at least one second stage processing element; and
> a first stage memory unit that is searched in response to search information from the first stage processing element;
> wherein the first and second stage processing elements are configured to allow the second stage processing element to perform search-independent processing related to a packet in parallel with a search of the first stage memory unit, where the search is related to the same packet.
> (Emphasis added.)

Claim 12 is patentable over the combination of Key and Rhoades for at least two reasons. First, the Examiner does not establish a *prima facie* rejection based on the combination of Key and Rhoades because the Examiner does not provide articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. Second, the combination of Key and Rhoades does not teach all of the limitations of the claim.

1. The Examiner does not establish a *prima facie* rejection based on the combination of Key and Rhoades because the Examiner does not provide articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

Prior to the Examiner's Answer, the Examiner did not establish a *prima facie* rejection based on the combination of Key and Rhoades because the Examiner did not

provide articulated reasoning with some rational underpinning to address the "same packet" language of the claim. As explained in Appellant's Appeal Brief, in order to establish a *prima facie* rejection of a claim under 35 U.S.C. 103, the Examiner must present a clear articulation of the reason why the claimed invention would have been obvious. MPEP 2142 (citing *KSR International Co. v. Teleflex Inc.*, 550 U.S. __ (2007)). The analysis must be made explicit. Id. Additionally, rejections based on obviousness cannot be sustained by mere conclusory statements; instead there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. Id.

In the Examiner's Answer, the Examiner states:

> **In response to Appellants argument in sub-section (1)**, Fig. 8 of Rhoades is self-explanatory for one of ordinary skill in the art that *Perform Table Lookup* is performed in parallel with *Transmission Error Detection-Packet Lifetime Calculations* [with] respect to the same packet. It would be meaningless for *Transmission Error Detection-Packet Lifetime Calculations* and *Perform Table Lookup* to merge into *Process Lookup Result* for a packet if the *Lookup Result* is for a different packet.
>
> Examiner's Answer, 10/26/09, pages 12-13 (emphasis in original).

To the extent that this might be considered articulated reasoning, it should be noted that this is the first time that the Examiner has presented such reasoning. In light of the Examiner's newly stated reasoning, Appellant withdraws the assertion that the Examiner has not established a *prima facie* rejection based on the failure to the "same packet" language of the claim.

Although the Examiner appears to address the "same packet" language of the claim, on its face, the Examiner nevertheless does not establish a *prima facie* rejection because the Examiner's reasoning is not rationally tied to the technical teachings of the proposed combination of cited references. In support of the rejection based on the combination f Key and Rhoades, the Examiner states:

> It would have been obvious to one of ordinary skill in the art at the time of the [sic] invention was made to have the first and second stage processing elements are [sic] configured to allow the second stage processing element

> to perform search-independent processing related to a packet in parallel with a search of the first stage memory unit, where the search is related to the same packet in order to provide the optimal balance between the conflicting demands of speed and programmability (Paragraph 16, Rhoades).
>
> Examiner's Answer, 10/26/09, page 4 (underlining added).

Even though Rhoades describes a data processing architecture that purportedly provides "the optimal balance between the conflicting demands of speed and programmability" (Rhoades, paragraph 16), the mere recitation of this language from Rhoades does not provide any rational underpinning to show how to incorporate the operations of Fig. 8 of Rhoades into the arrayed processing engine of Key in order to achieve an optimal balance between speed and programmability within the arrayed processing engine of Key. More specifically, the mere assertion that combining Rhoades and Key might achieve better speed and performance in the system of Key does not provide any rationale to show a connection between the parallel operations of Rhoades and the stated balance between speed and performance.

Furthermore, it should be noted that the balance of speed and performance described in Rhoades appears to rely on three criteria, including 1) the speed of logic, 2) the programmability of a CPU, and 3) fast access to large amounts of local memory. Rhoades, paragraph 10. However, the Examiner does not attempt to explain how performing a table lookup operation in parallel with other operations (i.e., transmission error detection through packet lifetime calculations of Fig. 8) might contribute to these three criteria. In the absence of some explanation from the Examiner to identify how the description of Fig. 8 might contribute to these three criteria for balancing speed and performance, there appears to be no connection between the operations illustrated in Fig. 8 and the ability of the data processing architecture, as a whole, to achieve a balance of speed and performance.

Therefore, the reasoning presented in the rejection is insufficient to establish a *prima facie* rejection because the Examiner's reasoning is not rationally tied to specific technical teachings that might achieve the asserted balance of speed and power.

Additionally, the Examiner's reasoning does not provide a rational explanation of how the parallel operations of Rhoades might be incorporated into the arrayed processing engine of Key in order to achieve an optimal balance between speed and programmability within the arrayed processing engine of Key. Accordingly, Appellant respectfully requests that the rejection of claim 12 under 35 U.S.C. 103(a) be withdrawn because the Examiner fails to establish a *prima facie* rejection.

2. The combination of Key and Rhoades does not teach all of the limitations of the claim.

Claim 12 is also patentable over the combination of Key and Rhoades because the combination of Key and Rhoades does not teach all of the limitations of the claim. In particular, the combination of Key and Rhoades does not teach a second stage processing element that performs search-independent processing in parallel to the first stage memory unit.

As a preliminary matter, Appellants appreciate the Examiner's clarification regarding the asserted correlation between the teachings of Rhoades and the limitations recited in the claim. For reference, the figure below replicates Fig. 8 of Rhoades and includes annotations to show the operations that purportedly correspond to the limitations recited in the claim.

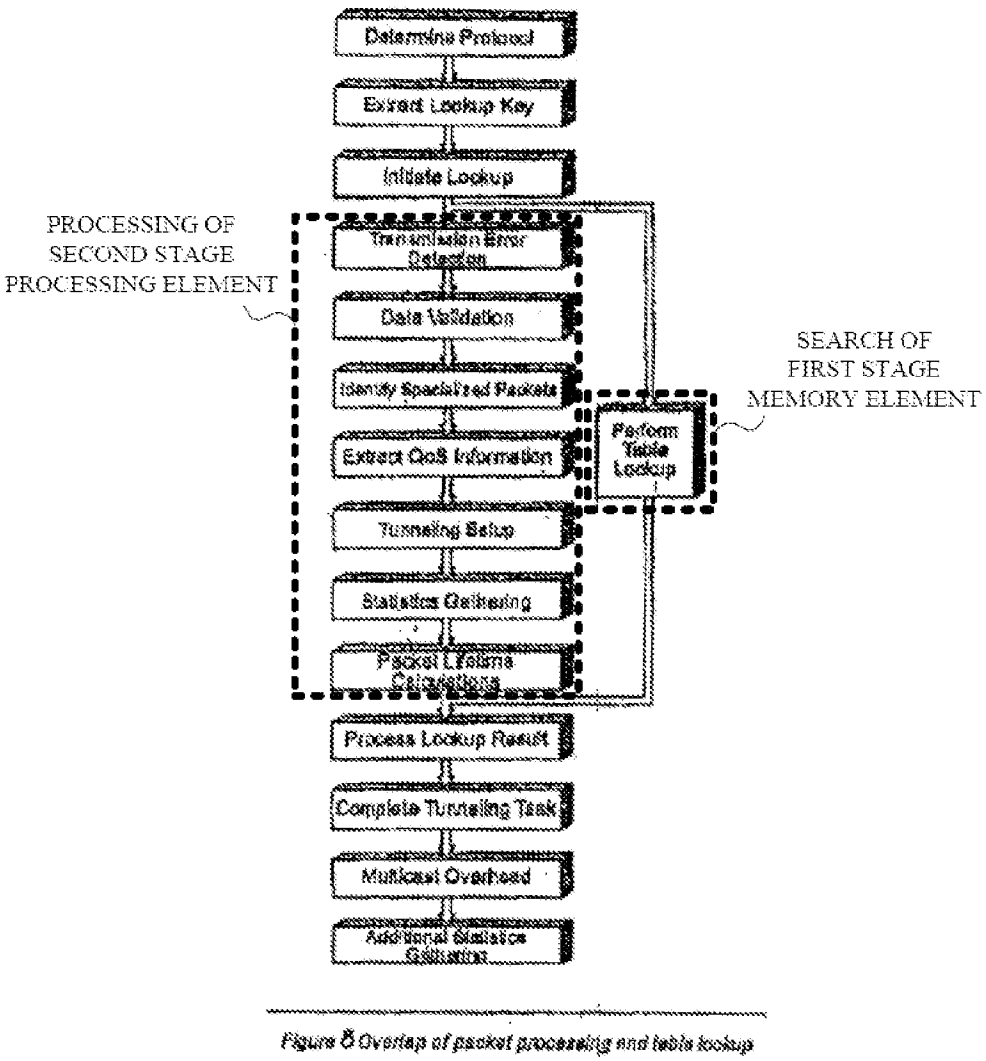

Fig. 8 of Rhoades with annotations based on the Examiner's assertions.

Although the Examiner asserts that performing the table lookup corresponds to the recited first stage memory unit and performing the other operations in parallel corresponds to the recited second stage processing element, this assertion is not supported by the actual disclosure of Rhoades. In particular, there is no correlation between the method operations described in Rhoades and specific processing stages, processing elements, or memory units corresponding to such processing elements. Also, Rhoades does not teach searching a first stage memory unit.

a. The method operations of Rhoades do not correlate to specific processing elements, or stages, or corresponding memory units.

Rhoades does not describe any correlation between the method operations of Fig. 8 and the individual processing elements (PEs). Rhoades merely state:

> The threads are structured so as to maximise the overlap of operations. FIG. 8 illustrates the overlap between packet processing and table lookup for a single processor. The processors synchronise with ocher [sic] processors and hardware accelerators via semaphores. In this example the global semaphores are used to keep the processors in step with one another but out of phase.
>
> Rhoades, paragraph 349 (underlining added).

Although Rhoades describes the operations of a single processor, generally, Rhoades does not describe the operations of separate PEs or pipeline stages within a processor. Moreover, although each processor contains an array of identical, small, efficient PEs (Rhoades, paragraphs 45 and 203; Fig. 4), the general description from Rhoades that is relied on by the Examiner does not provide any basis to presume that the various method operations of Fig. 8 might be implemented by different PEs or pipeline stages. Thus, the general description of some of the functionality of a single processor, without specific reference to any of the PEs arrayed within the processor, is insufficient to disclose functionality of specific PEs within the processor.

Therefore, the combination of Key and Rhoades does not teach all of the limitations of claim 12 because Rhoades merely describes general operations of a single processor, but does not disclose specific functionality of the individual PEs within the processor. Accordingly, Appellant respectfully asserts independent claim 12 is patentable over the combination of Key and Rhoades because the combination of Key and Rhoades does not teach all of the limitations of the claim.

b. Rhoades does not teach searching a first stage memory unit.

Also, as a separate basis for patentability, Rhoades does not teach searching a first stage memory unit. Rhoades merely describes a table lookup operation (see Fig. 8) that is performed by a common, shared table lookup engine (see Fig. 6) that is part of the network processor (which is different from the MTAP processors which implement the array of PEs). For reference, the figure below replicates Fig. 6 of Rhoades to show the shared table lookup engine(s) relative to the MTAP processor(s).

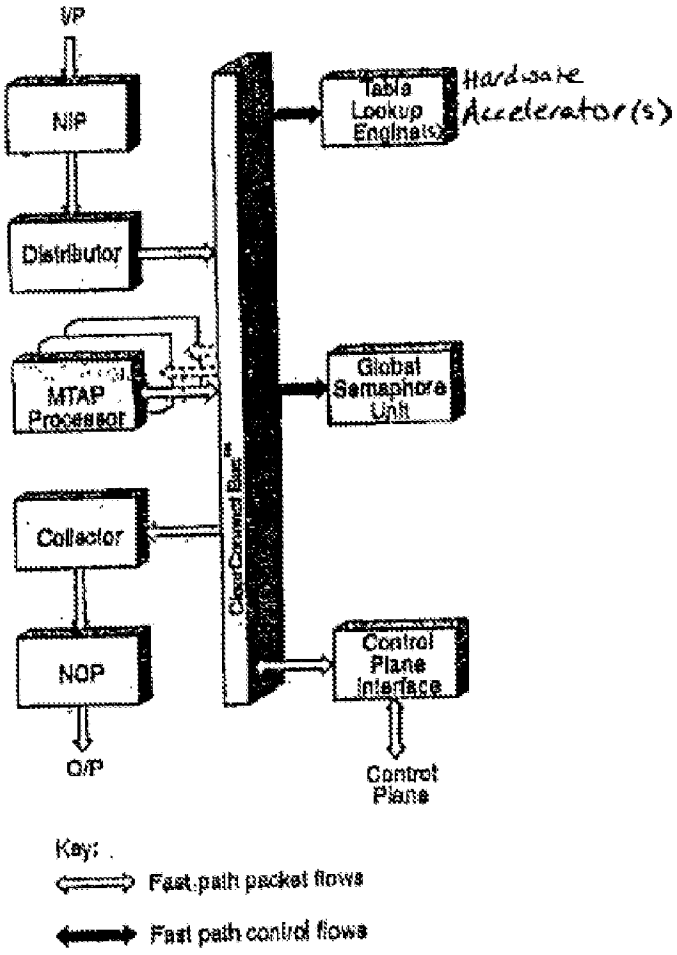

Figure 6 Example fast path processing subsystem

Fig. 6 of Rhoades to show the shared table lookup engine(s) relative to the MTAP processor(s).

While the data processing architecture of Rhoades may implement more than one table lookup engine or corresponding memory device, Rhoades does not describe any correlation between the table lookup engine(s) or memory devices and the PEs implemented within the MTAP processors. More specifically, Rhoades does not disclose any type of first stage memory unit which corresponds to a "first stage" of a pipeline or a "first stage" PE within a particular MTAP processor, regardless of the type of memory devices that might be connected to the various table lookup engine(s). Thus, the description in Rhoades of using common, shared table lookup engine(s), without some type of correlation between corresponding memory devices and specific PEs or stages within a MTAP processor, is insufficient to disclose searching a first stage memory unit.

Therefore, the combination of Key and Rhoades does not teach all of the limitations of claim 12 because Rhoades merely describes using common, shared table lookup engine(s), but does not disclose searching a "first stage" memory device that corresponds to a "first stage" of a pipeline or a "first stage" PE. Accordingly, Appellant respectfully asserts independent claim 12 is patentable over the combination of Key and Rhoades because the combination of Key and Rhoades does not teach all of the limitations of the claim.

B. Claims 1, 2, and 3 are patentable over the combination of Rhoades and Van Lunteren because the combination of cited references does not teach all of the limitations of the claims.

Claims 1, 2, and 3 are patentable over the combination of Rhoades and Van Lunteren because the combination of cited references does not teach all of the limitations of the claims. Claim 1 recites:

> A method for processing packet information using an array of processing elements comprising:
>
> performing a first search using a first stage processing element related to a packet using first search information;
>
> performing, in parallel with the first search, search-independent processing using a second stage processing element on information related to the packet; and

performing search-dependent processing using a result from the first search and a result of the search-independent processing to produce second search information.

(Emphasis added.)

Appellant respectfully asserts independent claim 1 is also patentable over the combination of Rhoades and Van Lunteren for at least one or more similar reasons to those stated above in regard to the rejection of independent claim 12. Although the language of claim 1 differs from the language of claim 12, and the scope of each claim should be interpreted independently of other claims, Appellant respectfully asserts that the remarks provided above in regard to the rejection of claim 12 also apply to the rejection of claim 1. Accordingly, Appellant respectfully asserts independent claim 1 is patentable over the combination of Rhoades and Van Lunteren because the combination of references does not teach the indicated limitations.

Given that claims 2 and 3 depend from and incorporate all of the limitations of the corresponding independent claim 1, which is patentable over the combination of Rhoades and Van Lunteren, Appellant respectfully submits that dependent claims 2 and 3 are also patentable over the cited references based on an allowable base claim. Additionally, each of claims 2 and 3 may be allowable for further reasons. Accordingly, Appellant requests that the rejections of claims 1, 2, and 3 under U.S.C 103(a) be withdrawn.

C. Claims 6, 7, 11, 14, and 15 are patentable over the combination of Key, Rhoades, and Van Lunteren because the combination of cited references does not teach all of the limitations of the claims.

Appellant respectfully submits that claim 6 is patentable over the combination of Key, Rhoades, and Van Lunteren because the combination of references does not teach all of the limitations of the claim. Claim 6 recites:

A method for processing packet information comprising:

processing information related to a packet using a first stage processing element to produce a first search key, wherein the first stage processing element is included within an array of processing elements;

searching a first stage memory unit using the first search key;

performing, in parallel with the search of the first stage memory unit, search-independent processing on information related to the packet using a

second stage processing element, wherein the second stage processing element is included within the array of processing elements;

performing, at the second stage processing element, search-dependent processing using a result from the search of the first stage memory unit and a result of the search-independent processing to produce a second search key; and

searching a second stage memory unit using the second search key.

(Emphasis added.)

Appellant respectfully asserts independent claim 6 is also patentable over the combination of Key, Rhoades, and Van Lunteren for at least one or more similar reasons to those stated above in regard to the rejection of independent claim 12. Although the language of claim 6 differs from the language of claim 12, and the scope of each claim should be interpreted independently of other claims, Appellant respectfully asserts that the remarks provided above in regard to the rejection of claim 12 also apply to the rejection of independent claim 6. Accordingly, Appellant respectfully asserts independent claim 6 is patentable over the combination of Key, Rhoades, and Van Lunteren because the combination of Key, Rhoades, and Van Lunteren does not teach the indicated limitations.

Given that claims 7, 11, 14, and 15 depend from and incorporate all of the limitations of the corresponding independent claims 6 and 12, which are patentable over the combination of Key, Rhoades, and Van Lunteren, Appellant respectfully submits that dependent claims 7, 11, 14, and 15 are also patentable over the cited references based on an allowable base claim. Additionally, each of claims 7, 11, 14, and 15 may be allowable for further reasons. Accordingly, Appellant requests that the rejections of claims 6, 7, 11, 14, and 15 under U.S.C 103(a) be withdrawn.

D. Claims 13, 17, 18, 20, and 21 are patentable over the combination of Key, Rhoades, and Kaganoi because the combination of cited references does not teach all of the limitations of the claims.

Appellant respectfully submits that claim 18 is patentable over the combination of Key, Rhoades, and Van Lunteren because the combination of references does not teach all of the limitations of the claim. Claim 18 recites:

A system for processing packet information comprising:
an array of processing elements having;
a plurality of first stage processing elements; and
a plurality of second stage processing elements; and
a memory interface that is configured to provide search information to a first stage memory unit from the plurality of first stage processing elements and to provide search results from the first stage memory unit directly to the plurality of second stage processing elements, wherein the first and second stage processing elements are configured to allow the second stage processing elements to perform search-independent processing related to respective packets in parallel with searches of the first stage memory unit, where the searches are related to the same packets.
(Emphasis added.)

Appellant respectfully asserts independent claim 18 is also patentable over the combination of Key, Rhoades, and Kaganoi for at least one or more similar reasons to those stated above in regard to the rejection of independent claim 12. Although the language of claim 18 differs from the language of claim 12, and the scope of each claim should be interpreted independently of other claims, Appellant respectfully asserts that the remarks provided above in regard to the rejection of claim 12 also apply to the rejection of independent claim 18. Accordingly, Appellant respectfully asserts independent claim 18 is patentable over the combination of Key, Rhoades, and Kaganoi because the combination of Key, Rhoades, and Kaganoi does not teach the indicated limitations.

Given that claims 13, 17, 20, and 21 depend from and incorporate all of the limitations of the corresponding independent claims 12 and 18, which are patentable over the combination of Key, Rhoades, and Kaganoi, Appellant respectfully submits that dependent claims 13, 17, 20, and 21 are also patentable over the cited references based on allowable base claims. Additionally, each of claims 13, 17, 20, and 21 may be allowable for further reasons. Accordingly, Appellant requests that the rejections of claims 13, 17, 18, 20, and 21 under U.S.C 103(a) be withdrawn.

E. Claims 4 and 5 are patentable over the combination of Rhoades, Van Lunteren, and Khanna because the combination of cited references does not teach all of the limitations of the claims.

Given that claims 4 and 5 depend from and incorporate all of the limitations of the corresponding independent claim 1, which are patentable over the combination of Rhoades, Van Lunteren, and Khanna, Appellant respectfully submits that dependent claims 4 and 5 are also patentable over the cited references based on an allowable base claim. Additionally, each of claims 4 and 5 may be allowable for further reasons. Accordingly, Appellant requests that the rejections of claims 4 and 5 under U.S.C 103(a) be withdrawn.

F. Claim 10 is patentable over the combination of Key, Rhoades, Van Lunteren, and Khanna because the combination of cited references does not teach all of the limitations of the claim.

Given that claim 10 depends from and incorporates all of the limitations of the corresponding independent claim 6, which is patentable over the combination of Key, Rhoades, Van Lunteren, and Khanna, Appellant respectfully submits that dependent claim 10 is also patentable over the cited references based on an allowable base claim. Additionally, claim 10 may be allowable for further reasons. Accordingly, Appellant requests that the rejection of claim 10 under U.S.C 103(a) be withdrawn.

G. Claims 8 and 9 are patentable over the combination of Key, Rhoades, Van Lunteren, and Kaganoi because the combination of cited references does not teach all of the limitations of the claims.

Given that claims 8 and 9 depend from and incorporate all of the limitations of the corresponding independent claim 6, which is patentable over the combination of Key, Rhoades, Van Lunteren, and Kaganoi, Appellant respectfully submits that dependent claims 8 and 9 are also patentable over the cited references based on an allowable base claim. Additionally, claims 8 and 9 may be allowable for further reasons. Accordingly, Appellant requests that the rejections of claims 8 and 9 under U.S.C 103(a) be withdrawn.

IV. CONCLUSION

For the reasons stated above, claims 1-15, 17, 18, 20, and 21 are patentable over the cited references. Thus, the rejections of claims 1-15, 17, 18, 20, and 21 should be withdrawn. Appellant respectfully requests that the Board reverse the rejections of claims 1-15, 17, 18, 20, and 21 under 35 U.S.C. 103(a) and, since there are no remaining grounds of rejection to be overcome, direct the Examiner to enter a Notice of Allowance for claims 1-15, 17, 18, 20, and 21.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-3444** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-3444** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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V. CLAIMS APPENDIX

1. A method for processing packet information using an array of processing elements comprising:

performing a first search using a first stage processing element related to a packet using first search information;

performing, in parallel with the first search, search-independent processing using a second stage processing element on information related to the packet; and

performing search-dependent processing using a result from the first search and a result of the search-independent processing to produce second search information.

2. The method of claim 1 further including performing a second search using the second search information.

3. The method of claim 2 further including holding a processing state from the search-independent processing until the result from the first search is available.

4. The method of claim 2 wherein performing search-dependent processing to produce the second search information includes producing a comparand and a mask as the second search information.

5. The method of claim 4 wherein performing the second search includes searching a content addressable memory using the comparand and the mask.

6. A method for processing packet information comprising:

processing information related to a packet using a first stage processing element to produce a first search key, wherein the first stage processing element is included within an array of processing elements;

searching a first stage memory unit using the first search key;

performing, in parallel with the search of the first stage memory unit, search-independent processing on information related to the packet using a second stage

processing element, wherein the second stage processing element is included within the array of processing elements;

performing, at the second stage processing element, search-dependent processing using a result from the search of the first stage memory unit and a result of the search-independent processing to produce a second search key; and

searching a second stage memory unit using the second search key.

7. The method of claim 6 further including holding a processing state from the search-independent processing until the result from the search of the first stage memory unit is received at the second stage processing element.

8. The method of claim 7 further including providing the result from the search of the first stage memory unit directly to the second stage processing element from the first stage memory unit.

9. The method of claim 6 further including providing the result from the search of the first stage memory unit directly to the second stage processing element from the first stage memory unit.

10. The method of claim 6 wherein the first and second search keys include a comparand and a mask.

11. The method of claim 6 further including forwarding information related to the packet to the second stage processing element before the result from the search of the first stage memory is produced.

12. A system for processing packet information comprising:

an array of processing elements having;

at least one first stage processing element; and

at least one second stage processing element; and

a first stage memory unit that is searched in response to search information from the first stage processing element;

wherein the first and second stage processing elements are configured to allow the second stage processing element to perform search-independent processing related to a packet in parallel with a search of the first stage memory unit, where the search is related to the same packet.

13. The system of claim 12 further including a direct communications link between the first stage memory unit and the second stage processing element configured to provide search results directly to the second stage processing element from the first stage memory unit.

14. The system of claim 12 wherein the second stage processing element is further configured to perform search-dependent processing using a result of the search of the first stage memory unit and a result from the search-independent processing to produce a search key.

15. The system of claim 14 further including a second stage memory unit that is associated with the second stage processing element, wherein the search key is used to search the second stage memory unit.

16. The system of claim 15 further including at least one third stage processing element, wherein the second and third stage processing elements are configured to allow the third stage processing element to perform search-independent processing related to the packet in parallel with the search of the second stage memory unit.

17. The system of claim 12 wherein the first stage memory unit comprises content addressable memory.

18. A system for processing packet information comprising:

an array of processing elements having;

a plurality of first stage processing elements; and

a plurality of second stage processing elements; and

a memory interface that is configured to provide search information to a first stage memory unit from the plurality of first stage processing elements and to provide search results from the first stage memory unit directly to the plurality of second stage processing elements, wherein the first and second stage processing elements are configured to allow the second stage processing elements to perform search-independent processing related to respective packets in parallel with searches of the first stage memory unit, where the searches are related to the same packets.

19. (canceled)

20. The system of claim 18 wherein the first stage processing elements forward information to respective second stage processing elements before results from respective searches of the first stage memory unit are received by the second stage processing elements.

21. The system of claim 18 further including:

a first bus that connects the plurality of first stage processing elements to the memory interface; and

a second bus that connects the plurality of second stage processing elements to the memory interface.